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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/750,021	JUNG ET AL.	
	Examiner	Art Unit	
	Quovaunda Jefferson	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *March 1, 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6 and 8-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 8-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 21-26 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Table 1 on page 16 and 17 and page 18 of Specification lists EOPs, end of points or etch stop points, with a the symbol after a number, i.e. an EOP of 25" or 0". However, it is unclear as to exactly how this EOP standard is determined and measured.

While it is known in the US Measurement Standard that the symbol ' " ' after a numerical value represents a measurement in terms of "inches", it is not possibly not the application, since etching semiconductor is performed at a nanoscale measurement. The Specification lacks a description that set forth how to measure the EOP or what parameters are involved in determining the EOP. For example, while page 18, line 13 of the Specification states "about 5", about 0" and about 0" "as different amounts of etching times. However, it is unclear as to what steps and parameters are involved at arriving to this specific EOP values. Are these EOP values, for example, etching times which are determined by a length of time required to etch to a certain distance, and if so how would this distance be measured? Or, are these values determined by another different of parameters that have not been set forth yet?

Claims 21-26 are rejected under 35 U.S.C. 112, first paragraph, as based on a disclosure which is not enabling.

The parameters or description on how to determine the EOP of an angle are critical or essential to the practice of the invention, but not included in the claim(s) is not enabled by the disclosure. See *In re Mayhew*, 527 F.2d 1229, 188 USPQ 356 (CCPA 1976).

The Specification lacks a description that set forth how to measure the EOP or what parameters are involved in determining the EOP. For example, while page 18, line 13 of the Specification states "about 5", about 0" and about 0" "as different amounts of etching times. However, it is unclear as to what steps and parameters are involved at arriving to this specific EOP values. Are these EOP values, for example, etching times which are determined by a length of time required to etch to a certain distance, and if so how would this distance be measured? Or, are these values determined by another different of parameters that have not been set forth yet?

Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The term "common condition" in claim 1 is a relative term, which renders the claim indefinite. The term "common conditions" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. It is unclear as to exact atmosphere parameters or conditions are considered "common" or possibly "uncommon".

Claims 21-27 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Where applicant acts as his or her own lexicographer to specifically define a term of a claim contrary to its ordinary meaning, the written description must clearly redefine the claim term and set forth the uncommon definition so as to put one reasonably skilled in the art on notice that the applicant intended to so redefine that claim term. *Process Control Corp. v. HydReclaim Corp.*, 190 F.3d 1350, 1357, 52 USPQ2d 1029, 1033 (Fed. Cir. 1999). The symbol " " " in claims 21-27 is used by the claim to mean "etching times", while the accepted meaning in US Measurements is "inches." The term is indefinite because the specification does not clearly redefine the term.

Claims 22 and 25 recite the limitation "...a pressure of about 10mtorr..." However, claims 21 and 24, on which claims 22 and 25 are dependent upon, respectively, recite "...a pressure of 88 mmtorr..." It is unclear as to how the pressure would exist at both of these different and distinct values.

Claims 22 and 25 recite the limitation "...a source power of about 1000 W..." However, claims 21 and 24, on which claims 22 and 25 are dependent upon, respectively, recite "...a source power of about 600W..." It is unclear as to how the source power would exist at both of these different and distinct values.

Claims 22 and 25 recite the limitation "...etching times of about 5", about 0", and about 0"...." However, claims 21 and 24, on which claims 22 and 25 are dependent upon, respectively, recite "...etching times of about 0", about 10", and about 0"..." It is unclear as to how both etching times would occur at two different and distinct values.

Claims 23 and 26 recite the limitation "...a power of 600W..." However, claims 22 and 25, on which claims 23 and 26 are dependent upon, respectively, recite "...a source power of 1000W..." It is unclear as to how the power would exist at both of these different and distinct values.

Claims 23 and 26 recite the limitation "...a bias power of about 275 W..." However, claims 22 and 25, on which claims 23 and 26 are dependent upon, respectively, recite "...a bias power of about 90W..." It is unclear as to how the bias power would exist at both of these different and distinct values.

Claims 23 and 26 recite the limitation "...a CF_4 with about 80 sccm..." However, claims 21 and 24, on which claims 23 and 26 are ultimately dependent upon, recite "...a CF_4 with about 50 sccm..." It is unclear as to how the bias power would exist at both of these different and distinct values.

Claims 23 and 26 recite the limitation "...etching times of about 0", about 7"', and about 7..." However, claims 22 and 25, on which claims 23 and 26 are dependent upon, respectively, recite "...etching times of about 5", about 0", and about 0"..." It is unclear as to how both etching times would occur at two different and distinct values.

Claims 21-27 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential steps, such omission amounting to a gap between the steps. See MPEP § 2172.01.

The omitted steps are the steps needed to determine or measure the EOP or what parameters are involved in determining the EOP.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 9, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Park et al, US Patent 6,465,866 (as cited in a previous office action) in view of Gupta et al, US Patent 5,746,884.

3. Regarding claim 1, Park teaches A method for forming a device isolation layer of a semiconductor device, comprising the steps of forming a pad layer pattern **42, 44** defining a device isolation layer on a substrate **40**, wherein the pad layer pattern includes a pad oxide layer **42** and a pad nitride layer **44**, forming a trench **47** by etching an exposed portion of the substrate with use of the pad layer pattern as a mask, performing an etching process to make top corners of the trench rounded under a predetermined common condition (figure 5E), forming a lateral oxide layer **48** on a partial surface of the substrate, the partial surface consisting of sidewalls and a bottom area in the trench by a dry oxidation technique, wherein the dry oxidation technique oxidates the sidewalls and bottom area in the trench formed by the etching process (Note: from the etching process of forming trench **47**), forming a liner nitride layer **50** on the lateral oxide layer, forming an insulation layer **52** on the liner nitride layer to fill the trench, planarizing the insulation layer until the pad nitride layer is removed, and removing the pad oxide layer (Figures 5A-5E).

Park fails to teach performing an etching process to make top corners of the trench rounded by controlling an angle of the top corners of the trench wherein angles of about 30°, about 45°, and about 90° of the top corners are made in response to a different etching time.

Gupta teaches performing an etching process to make top corners of the trench rounded by controlling an angle of the top corners of the trench wherein angles of about 30°, about 45°, and about 90° of the top corners are made in response to a different etching time (column 4, lines 38-62) in a method of forming a fluted sidewall by adjusting the times of the appropriate etch steps, the via profile can be controlled to provide a gently sloping, substantially continuous sidewall extending from an upper surface of the dielectric layer to an upper surface of an underlying layer. The advantage of forming the fluted sidewall is to improve continuity of the sidewalls, which in turns, improves uniform coverage of subsequent interconnection layers deposited upon the etched trench walls, thereby increasing reliability of the semiconductor device, because an interconnection layer that has poor uniform coverage because electromigration in the narrow portions of the interconnect layer can eventually result in a highly resistive or open interconnect.

It would be obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Gupta with that of Park because the advantage of forming the fluted sidewall is to improve continuity of the sidewalls, which in turns, improves uniform coverage of subsequent interconnection layers deposited upon the etched trench walls, thereby increasing reliability of the semiconductor device, because an interconnection layer that has poor uniform coverage because electromigration in the narrow portions of the interconnect layer can eventually result in a highly resistive or open interconnect.

4. Regarding claim 4, Gupta teaches the etching process proceeds by employing an isotropic etching technique (column 1, line 58-67).

5. Regarding claim 5, Gupta teaches an angle of top corners of the trench is controlled through the use of the isotropic etching technique (column 1, lines 58-67 and column 3, lines 23-25).

6. Regarding claim 6, Gupta teaches the isotropic etching technique uses a gas containing CF_4 and 0_2 gas (column 3, lines 23-25).

7. Regarding claim 8, Park teaches the lateral oxide layer with a thickness ranging from about 60 A to about 100 A (column 5, line 58).

Park and Gupta fail to teach the dry oxidation technique is performed at a temperature of about 900°C to about 1000°C.

However, given the teaching of the references, it would have been obvious to determine the optimum condition of delivery of the layers involved. See *In re Aller, Lacey, and Hall* (10 USPQ 23 3-237) "It is not inventive to discover optimum or workable ranges by routine experimentation. Note that the specification contains no disclosure of ether the critical nature of the claimed ranges or any unexpected results

arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that tile chosen dimensions are critical. *In re Woodruff*, 919 f.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Any differences in the claimed invention and the prior art may be expected to result in some differences in properties. The issue is whether the properties differ to such an extent that the difference is really unexpected. *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Appellants have the burden of explaining the data in any declaration they proffer as evidence of non-obviousness. *Ex parte Ishizaka*, 24 USPQ2d 1621, 1624 (Bd. Pat. App. & Inter. 1992).

An Affidavit or declaration under 37 CFR 1.132 must compare the claimed subject matter with the closest prior art to be effective to rebut a prima facie case of obviousness. *In re Burckel*, 592 F.2d 1175, 201 USPQ 67 (CCPA 1979).

8. Regarding claim 9, Park teaches a method for fabricating a semiconductor device, comprising the steps of forming a pad oxide layer **42** and a pad nitride layer **44** defining a device isolation layer on a substrate **40**, forming a trench **47** of which top corners are rounded (figure 5E) by etching a surface of a substrate to a predetermined depth by controlling an angle of the top corners of the trench under a predetermined common condition, forming a lateral oxide layer **48** on a partial surface of the substrate,

the partial surface consisting of sidewalls and a bottom area of the trench by oxidating sidewalls of the trench and the bottom area in the trench formed by the etching process, forming a liner nitride layer **50** on the lateral oxide layer, forming an insulation layer **52**on the liner nitride layer to bury the trench, planarizing the insulation layer until the pad nitride layer is removed, removing the pad oxide layer until a surface of the substrate is exposed, forming an oxide layer **54** on the exposed surface of the substrate, and forming a conductive layer **56** for a gate electrode on an entire surface of a structure containing the oxide layer (figures 5A-5F).

Park fails to teach forming a trench with top corner rounded by controlling an angle of the top corners of the trench, wherein angles of angles of about 30°, about 45°, and about 90° of the top corners are made in response to a different etching time and performing an etching process to the trench so that the top corners of the trench become more rounded.

Gupta teaches forming a trench with top corner rounded by controlling an angle of the top corners of the trench, wherein angles of angles of about 30°, about 45°, and about 90° of the top corners are made in response to a different etching time and performing an etching process to the trench so that the top corners of the trench become more rounded (column 4, lines 38-62) in a method of forming a fluted sidewall by adjusting the times of the appropriate etch steps, the via profile can be controlled to provide a gently sloping, substantially continuous sidewall extending from an upper

surface of the dielectric layer to an upper surface of an underlying layer. The advantage of forming the fluted sidewall is to improve continuity of the sidewalls, which in turns, improves uniform coverage of subsequent interconnection layers deposited upon the etched trench walls, thereby increasing reliability of the semiconductor device, because an interconnection layer that has poor uniform coverage because electromigration in the narrow portions of the interconnect layer can eventually result in a highly resistive or open interconnect.

It would be obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Gupta with that of Park because the advantage of forming the fluted sidewall is to improve continuity of the sidewalls, which in turns, improves uniform coverage of subsequent interconnection layers deposited upon the etched trench walls, thereby increasing reliability of the semiconductor device, because an interconnection layer that has poor uniform coverage because electromigration in the narrow portions of the interconnect layer can eventually result in a highly resistive

9. Regarding claim 11, Park teaches the lateral oxide layer is formed through a dry oxidation technique (column 4, lines 55-59).

10. Regarding claim 12, Park teaches the screen oxide layer and the gate oxide layer are formed through a dry oxidation technique (column 4, lines 55-59 and column 6, lines 58-62).

11. Regarding claim 13, Park teaches the lateral oxide layer is formed with a thickness in a range from about 60 Angstroms to about 100 Angstroms (column 5, line 58).

Park and Gupta fail to teach the lateral oxide layer is formed at a temperature ranging from about 900°C to about 1000°C.

However, given the teaching of the references, it would have been obvious to determine the optimum condition of delivery of the layers involved. See *In re Aller, Lacey, and Hall* (10 USPQ 23 3-237) "It is not inventive to discover optimum or workable ranges by routine experimentation. Note that the specification contains no disclosure of ether the critical nature of the claimed ranges or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that tile chosen dimensions are critical. *In re* Woodruff, 919 f.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Any differences in the claimed invention and the prior art may be expected to result in some differences in properties. The issue is whether the properties differ to such an extent that the difference is really unexpected. *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Appellants have the burden of explaining the

data in any declaration they proffer as evidence of non-obviousness. *Ex parte Ishizaka*, 24 USPQ2d 1621, 1624 (Bd. Pat. App. & Inter. 1992).

An Affidavit or declaration under 37 CFR 1.132 must compare the claimed subject matter with the closest prior art to be effective to rebut a prima facie case of obviousness. *In re Burckel*, 592 F.2d 1175, 201 USPQ 67 (CCPA 1979).

12. Regarding claim 14, Park and Gupta fail to teach the screen oxide layer is formed at a temperature ranging from about 850°C to about 1000°C with a thickness in a range from about 50 Angstroms to about 150 Angstroms.

However, given the teaching of the references, it would have been obvious to determine the optimum thickness, temperature as well as condition of delivery of the layers involved. See *In re Aller, Lacey, and Hall* (10 USPQ 23 3-237) "It is not inventive to discover optimum or workable ranges by routine experimentation. Note that the specification contains no disclosure of ether the critical nature of the claimed ranges or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that tile chosen dimensions are critical. *In re Woodruff*, 919 f.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Any differences in the claimed invention and the prior art may be expected to result in some differences in properties. The issue is whether the properties differ to

such an extent that the difference is really unexpected. *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Appellants have the burden of explaining the data in any declaration they proffer as evidence of non-obviousness. *Ex parte Ishizaka*, 24 USPQ2d 1621, 1624 (Bd. Pat. App. & Inter. 1992).

An Affidavit or declaration under 37 CFR 1.132 must compare the claimed subject matter with the closest prior art to be effective to rebut a prima facie case of obviousness. *In re Burckel*, 592 F.2d 1175, 201 USPQ 67 (CCPA 1979).

13. Regarding claim 15, Park and Gupta fail to teach the gate oxide layer is formed at a temperature ranging from about 850°C to about 1000°C.

However, given the teaching of the references, it would have been obvious to determine the optimum thickness, temperature as well as condition of delivery of the layers involved See *In re Aller, Lacey, and Hall* (10 USPQ 23 3-237) "It is not inventive to discover optimum or workable ranges by routine experimentation. Note that the specification contains no disclosure of ether the critical nature of the claimed ranges or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that tile chosen dimensions are critical. *In re Woodruff*, 919 f.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Any differences in the claimed invention and the prior art may be expected to result in some differences in properties. The issue is whether the properties differ to such an extent that the difference is really unexpected. *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Appellants have the burden of explaining the data in any declaration they proffer as evidence of non-obviousness. *Ex parte Ishizaka*, 24 USPQ2d 1621, 1624 (Bd. Pat. App. & Inter. 1992).

An Affidavit or declaration under 37 CFR 1.132 must compare the claimed subject matter with the closest prior art to be effective to rebut a prima facie case of obviousness. *In re Burckel*, 592 F.2d 1175, 201 USPQ 67 (CCPA 1979).

14. Regarding claim 18, Gupta teaches making the top corners of the trench more rounded proceeds by employing an isotropic etching technique (column 1, lines 58-67 and column 3, lines 23-25).

15. Regarding claim 19, Gupta teaches the top corners of the trench is controlled through the use of the isotropic etching technique (column 1, lines 58-67 and column 3, lines 23-25).

16. Regarding claim 20, Gupta teaches the isotropic etching technique proceeds by using a gas containing CF_4 and 0_2 gas (column 1, lines 58-67 and column 3, lines 23-

25).

17. Regarding claims 21 and 24, Park and Gupta fail to teach if the predetermined common condition for over-etching the pad layer includes a pressure of about 88 mtorr, a power of about 600 W, a CF_4 with about 50 sccm, and an Ar with about 300 sccm, the angles of about 30°, about 45°, and about 90° of the top corners are made at different etching times of about 0", about 10", and about 0".

However, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose these particular dimensions because applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

18. Regarding claims 22 and 25, Park and Gupta fail to teach if the predetermined common condition includes a pressure of about 10mtorr, a source power of about 1000 W, a bias power of about 275 W, a HBr with about 40 sccm, a He with about 10 torr and a temperature of about 20 °C, the angles of about 30°, about 45°, and about 90° of the top corners are made at different etching times of about 5", about 0", and about 0".

However, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose these particular dimensions because applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

19. Regarding claims 23 and 26, Park and Gupta fail to teach if the predetermined common condition includes a pressure of about 10 mtorr, a power of about 600 W, a bias power of about 90 W, a CF4 with about 80 sccm, a He with about 10 torr, and a

temperature of about 20 °C, the angles of about 30°, about 45°, and about 90° of the top corners are made at different etching times of about 0", about 7"', and about 7".

However, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose these particular dimensions because applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

20. Claims 2 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Park and Gupta as applied to claims 1 and 9 above, and further in view of Yu et al, US Patent 5,801,083 (as cited in a previous office action).

21. Regarding claim 2, Park and Gupta fail to teach an angle of the top corners of the trench is controlled according to a contained quantity of hydrogen bromide and chlorine gas in an etching gas.

Yu teaches an angle of the top corners of the trench is controlled according to a contained quantity of hydrogen bromide and chlorine gas in an etching gas (column 3, lines 36-41) because the tapered or sloped edge of the trench can be controlled by the etching conditions such as gas ratio, pressure, and bias and forming a oxide layer by a dry oxidation technique, wherein the dry oxidation technique oxidates the sidewalls and a bottom area in the trench formed by the etching process.

It would be obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Yu with that of Park and Gupta because the tapered or sloped edge of the trench can be controlled by the etching conditions such as gas ratio, pressure, and bias and a method to provide an additional insulating barrier layer for the substrate and to aid in decreasing the sharpness of the trench corner since sharp corners of a trench will increase points of high stress, which decreases the reliability of the semiconductor device is disclosed.

22. Regarding claim 16, Park and Yu fail to teach at the step of forming the trench of which top corners are rounded, the top corners of the trench are rounded according to a

contained quantity of hydrogen bromide and chlorine gas in an etching gas.

Yu teaches at the step of forming the trench of which top corners are rounded, the top corners of the trench are rounded according to a contained quantity of hydrogen bromide and chlorine gas in an etching gas (column 3, lines 36-41) because the tapered or sloped edge of the trench can be controlled by the etching conditions such as gas ratio, pressure, and bias and forming a oxide layer by a dry oxidation technique, wherein the dry oxidation technique oxidates the sidewalls and a bottom area in the trench formed by the etching process.

It would be obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Yu with that of Park and Gupta because the tapered or sloped edge of the trench can be controlled by the etching conditions such as gas ratio, pressure, and bias and a method to provide an additional insulating barrier layer for the substrate and to aid in decreasing the sharpness of the trench corner since sharp corners of a trench will increase points of high stress, which decreases the reliability of the semiconductor device is disclosed.

23. Claims 3 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Park, Gupta, and Yu as applied to claims 2 and 16 above, and further in view of Downey et al, US Patent 2003/0092273 (as cited in a previous office action).

24. Regarding claim 3, Yu teaches the step of performing the etching process includes the steps of performing an etching process by using hydrogen bromide (column 3, lines 11-12), removing a native oxide layer formed after the etching process by using carbon tetrafluoride (CF_4) gas (column 3, lines 11-12), performing an etching process with use of a gas containing hydrogen bromide and chloride gas to form the trench with a predetermined depth (column 3, lines 35-37).

Park, Gupta and Yu fail to teach performing an etching process by using a gas containing CF_9 and oxygen (O_2) gas to purge the chloride gas from a chamber.

Downey teaches performing an etching process by using a gas containing CF_9 and oxygen (O_2) gas to purge the chloride gas from a chamber [0027] because it is known that traces of chlorine left behind in the reaction may result in a catalytic reaction with water left in the process an may result in the creation of harmful corroding species.

It would be obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Downey with that of Park, Gupta, and Yu because it is known that traces of chlorine left behind in the reaction may result in a catalytic reaction with water left in the process an may result in the creation of harmful corroding species.

25. Regarding claim 17, Yu further teaches the step of forming the trench further includes the steps of performing an etching process by using hydrogen bromide

(column 3, lines 11-12), removing a native oxide layer formed after the etching process by using CF_4 gas (column 3, lines 11-12), performing an etching process by using a gas containing hydrogen bromide and chlorine gas until the trench has a predetermined depth (column 3, lines 35-37).

Park, Gupta, and Yu fail to teach performing an etching process by using a gas containing CF_9 and oxygen (O_2) gas to purge the chloride gas from a chamber.

Downey teaches performing an etching process by using a gas containing CF_9 and oxygen (O_2) gas to purge the chloride gas from a chamber [0027] because it is known that traces of chlorine left behind in the reaction may result in a catalytic reaction with water left in the process an may result in the creation of harmful corroding species.

It would be obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Downey with that of Park, Gupta, and Yu because it is known that traces of chlorine left behind in the reaction may result in a catalytic reaction with water left in the process an may result in the creation of harmful corroding species.

26. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Park and Gupta as applied to claim 9 above, and further in view of Huang et al, US Patent 5,976,951 (as cited in a previous office action).

27. Regarding claim 10, Park teaches forming a gate oxide layer on an exposed surface of the substrate (figure 5E).

Park and Gupta fail to teach forming a screen oxide layer for a threshold voltage control on the substrate, implanting a dopant for a threshold voltage control by using the screen oxide layer as a mask, removing the screen oxide layer, and forming the gate oxide after removing the screen oxide layer.

Huang teaches forming a screen oxide layer **218** for a threshold voltage control on the substrate, implanting a dopant for a threshold voltage control by using the screen oxide layer as a mask, removing the screen oxide layer; and forming the gate oxide **220** after removing the screen oxide layer (figures 15-18 and column 4, lines 61-67) as a means for a channel region by implanting dopant into the substrate, which helps to control the current flow from the source to the drain of a semiconductor transistor.

It would be obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Huang with that of Park and Gupta because implanting ions into the channel region of transistor on a substrate helps to control the current flow from the source to the drain of a semiconductor transistor.

Response to Arguments

Applicant's arguments with respect to claims 1-6 and 8-26 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quovaunda Jefferson whose telephone number is 571-272-5051. The examiner can normally be reached on Monday through Friday, 7AM to 3:30PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

QVJ

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PRIMARY PATENT EXAMINER